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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s):	Zhiqun Chen et al.		
Assignee:	Sun Microsystems, Inc.		
Title:	OPTIMIZATION OF N-BASE TYPED ARITHMETIC EXPRESSIONS		
Serial No.:	10/686,513	Filing Date:	October 14, 2003
Patent No.:	7,316,007	Issued:	January 1, 2008
Examiner:	John Q. Chavis	Group Art Unit:	2193
Docket No.:	P-4171CNT2		

Monterey, CA
August 19, 2008

ATTENTION: CERTIFICATE OF CORRECTIONS BRANCH
COMMISSIONER FOR PATENTS
P.O. BOX 1450
ALEXANDRIA, VA 22313-1450

REQUEST FOR ENTRY OF CERTIFICATE OF CORRECTION

Sir:

Please enter the enclosed Certificate of Correction (PTO Form 1050) in the above patent.

The errors sought to be corrected were made by

[X] The Patent and Trademark Office as explained below. Thus, no fee is required for the Certificate of Correction pursuant to 37 CFR §1.322.

[ ] Applicant(s) (at least in part). See next section for explanation. This appropriate fee under 37 CFR §1.323 has been authorized below.

Attached as Exhibit A (2 pages) are the relevant pages of the Amendment dated February 1, 2007, which support the requested corrections to Claims 18 and 82, and show that the errors were made by the U.S. Patent and Trademark Office.

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As shown in Exhibit A, Lines 5 to 6 of originally numbered Claim 53 (renumbered in the Patent as Claim 18) read "said second processor comprises a Java Card™ Virtual Machine". The same lines in the patent at Column 21, Lines 35 to 36, read "said second processor comprises a Java CardtM Virtual Machine".

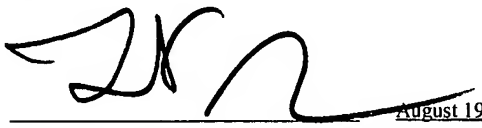
As also shown in Exhibit A, Line 4 of originally numbered Claim 117 (renumbered in the Patent as Claim 82) reads "...virtual machine executing a software application...". The same line in the patent at Column 28, Lines 1 to 2, reads "...virtualmachine executing a software application...".

Applicants respectfully request entry of the enclosed Certificate of Correction. The Commissioner is hereby authorized to charge any fees required for consideration and entry of the enclosed documents, and to credit any overpayment of fees to Deposit Account No. 50-0553.

Please direct all inquiries concerning this request to the undersigned attorney.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on August 19, 2008.



Attorney for Applicant(s) — August 19, 2008 — Date of Signature

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(Also Form PTO-1050)

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO : 7,316,007

APPLICATION NO. : 10/686,513

ISSUE DATE : January 1, 2008

INVENTOR(S) : Zhiqun Chen and Judith E. Schwabe

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Column 21, Claim 18, Line 35, replace "Java CardtM" with --Java Card™--.
In Column 28, Claim 82, Line 1, replace "virtualmachine" with --virtual machine--.

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discarding previous conversion results of said third instruction before said converting to a wider base.

48. (Previously Presented) The method of claim 46, further comprising rejecting an expression that cannot be optimized to a smaller base on said second processor.

49. (Previously Presented) The method of claim 46 wherein said converting to a wider base further comprises rejecting said first instruction when said wider base is not supported by said second processor.

50. (Previously Presented) The method of claim 46 wherein said first instruction is arithmetic.

51. (Previously Presented) The method of claim 46 wherein said first instruction comprises a non-arithmetic, type-sensitive instruction.

52. (Previously Presented) The method of claim 46, further comprising linking each instruction to successor instructions in all control paths.

53. (Previously Presented) The method of claim 46 wherein

said first processor comprises a Java™ Virtual Machine; and

~~said~~ second processor comprises a Java Card™ Virtual Machine.

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54. (Previously Presented) The method of claim 46 wherein

said first base is used by said first processor for performing arithmetic operations on at least one data

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Exhibit A

receiving a first instruction defined for a first processor having a first base, said instruction including an operator and at least one operand; and

converting said first instruction to a second instruction optimized for a second processor having a second base when said at least one operand does not carry potential overflow beyond said second base or when said operator is insensitive to overflow, said second base smaller than said first base;

the virtual machine comprising:

means for receiving optimized instructions, the optimized instructions being previously optimized for execution on a resource-constrained device; and

means for executing said instructions.

117. (Currently Amended) A smart card having a microcontroller embedded therein, the smart card comprising a virtual machine being executed by a microcontroller, the virtual machine executing a software application comprising of a plurality of previously optimized instructions, the instructions optimized by a method comprising:

receiving a first instruction defined for a first processor having a first base, said instruction including an operator and at least one operand; and

converting to a wider base a third instruction that is ~~the~~a source of potential overflow associated with said at least one operand when said at least one operand ~~carries~~ the potential for overflow beyond a second base of a second processor and when said operator is sensitive to overflow, said third instruction having been previously optimized, said second base smaller than said first base, said wider base larger than said second base and smaller or equal to said first base;

the virtual machine comprising:

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